IBM Systems and Technology Group

Designing low-frequency decoupling using SIMPLIS

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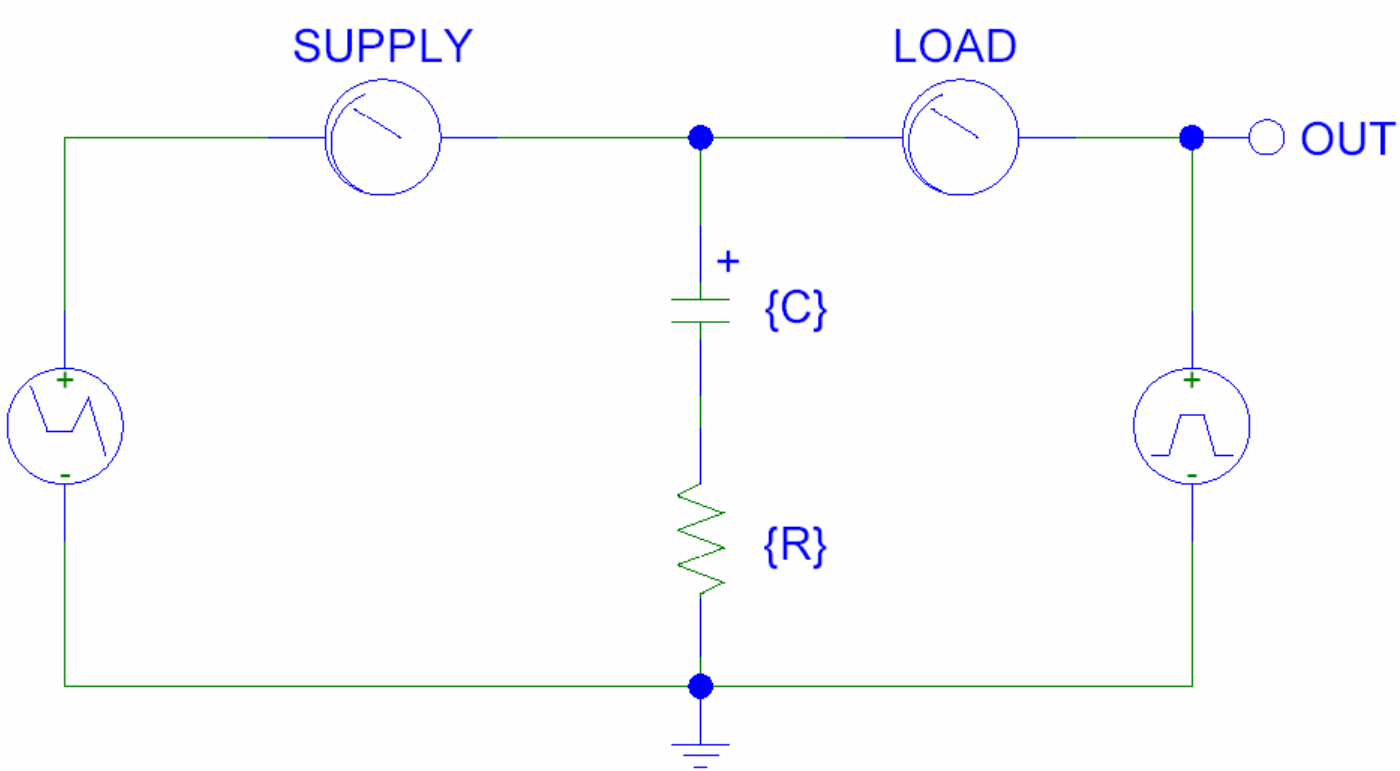
Traditional approach to sizing decoupling

- Determine effective ESR required
  - Parallel electrolytic caps until ESR = $\Delta V/\Delta I$

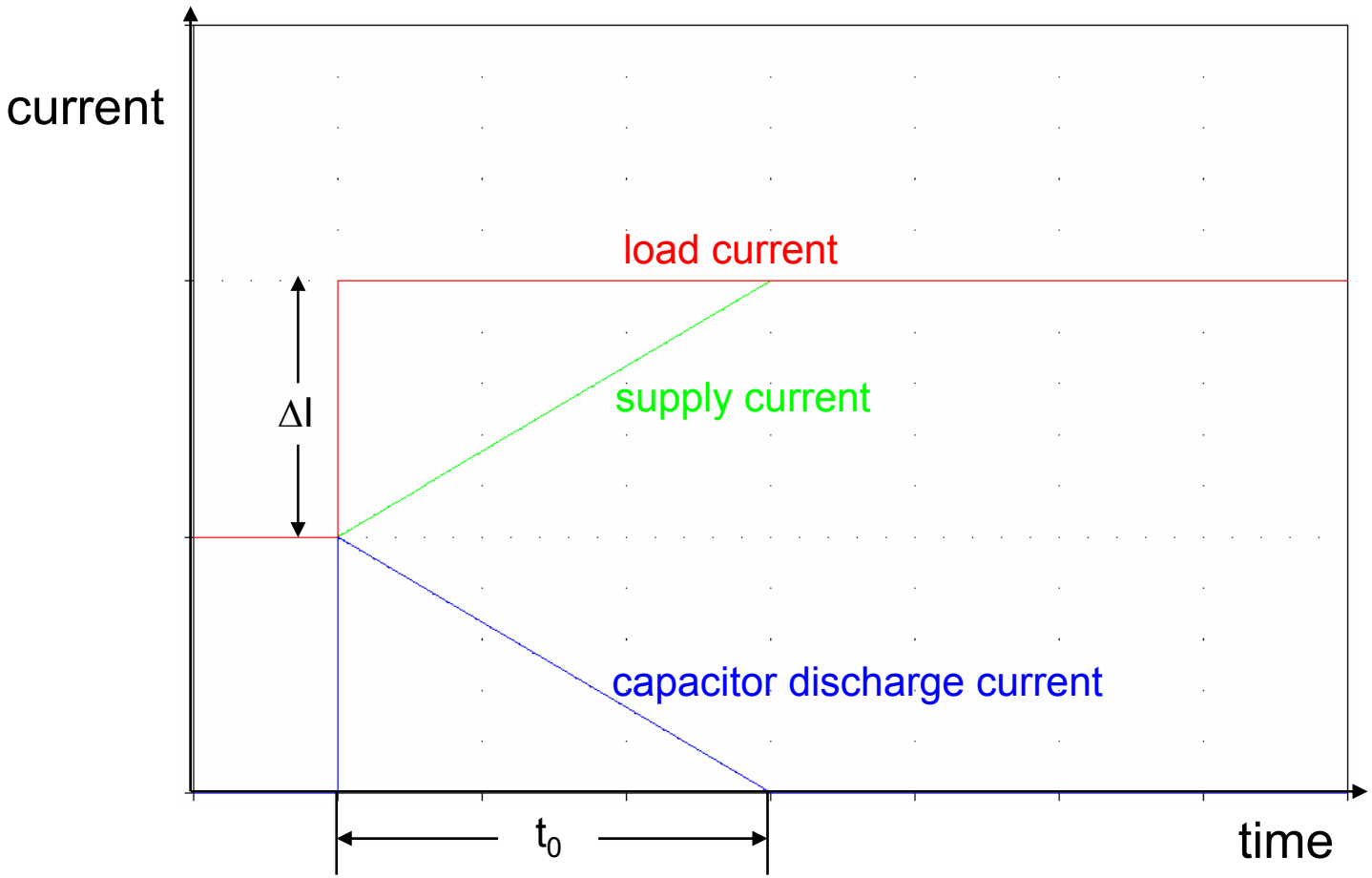
    where ΔV = desired voltage tolerance

    ΔI = worst-case load change
- Example: p690 Power 4 CPU
  - ΔV = 3% of 1.5V, ΔI = 1500A → effective ESR = 30uΩ
  - 2 capacitor books with over 800 1000uF aluminum electrolytic caps
  - CPU decoupling
    - 383 1000uF 38mΩ aluminum electrolytics per cap book → 50uΩ
    - 240 470uF 25mΩ organic Tantalum on processor board → 104uΩ
    - Effective ESR = 33.8uΩ max, typically much less

Simplified decoupling model



Current supplied by capacitor after a load step



Solve for maximum ΔV

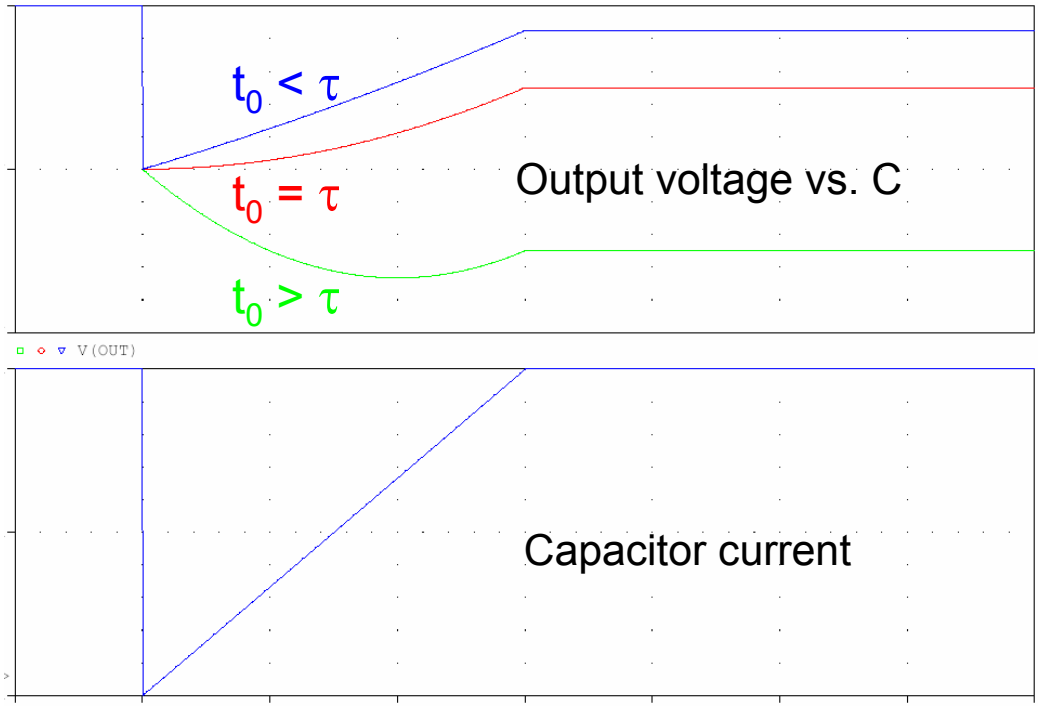
For $t_0 \leq \tau$:

$\Delta V = \Delta I \bullet R$

For $t_0 > \tau$:

$\Delta V = \Delta I \bullet (R/2) \bullet (\tau/t_0 + t_0/\tau)$

(τ = RC = capacitor time constant)



Response is limited by ESR!

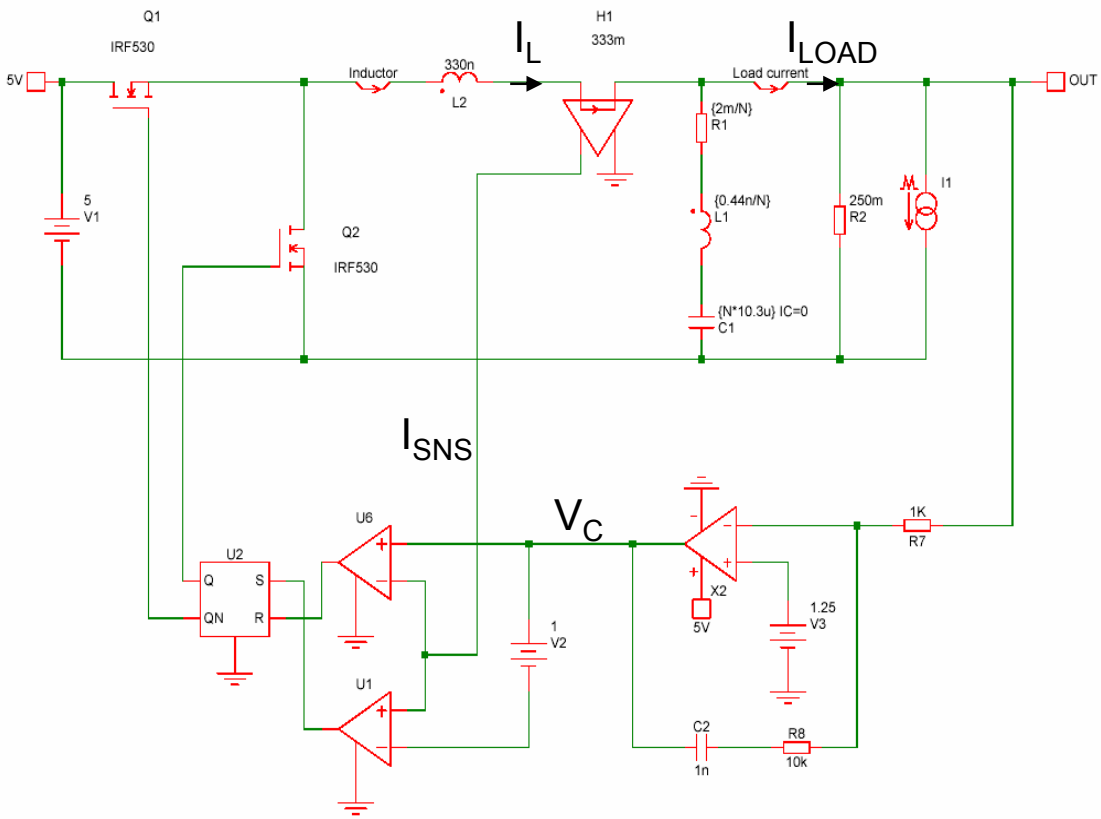
But it's not so simple anymore

- Denser packaging limits the number of output caps
  - Fewer caps with much lower ESR → shorter time constant
  - All multi-layer ceramic designs → very short time constant
- Result is that ESR no longer predicts ΔV
  - Regulator response time typically longer than RC time constant of decoupling caps ($t_0 > \tau$)
- Can use $\Delta V = \Delta I \cdot (R/2) \cdot (\tau/t_0 + t_0/\tau)$ equation, but how to determine t_0?
  - t_0 usually limited by feedback compensation

Computer modeling

- SPICE
  - Different models for transient and AC analysis
  - Full switching model is very slow
  - Convergence problems!!!
- SIMPLIS
  - Same model use for both transient and AC analysis
  - Up to 50x faster than SPICE simulators
  - No convergence problems

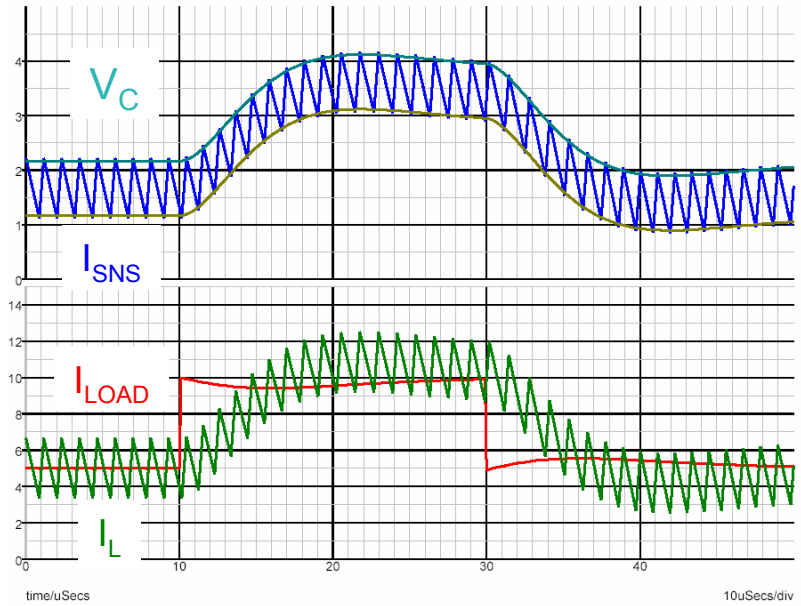
Current-Mode Hysteretic Buck Converter



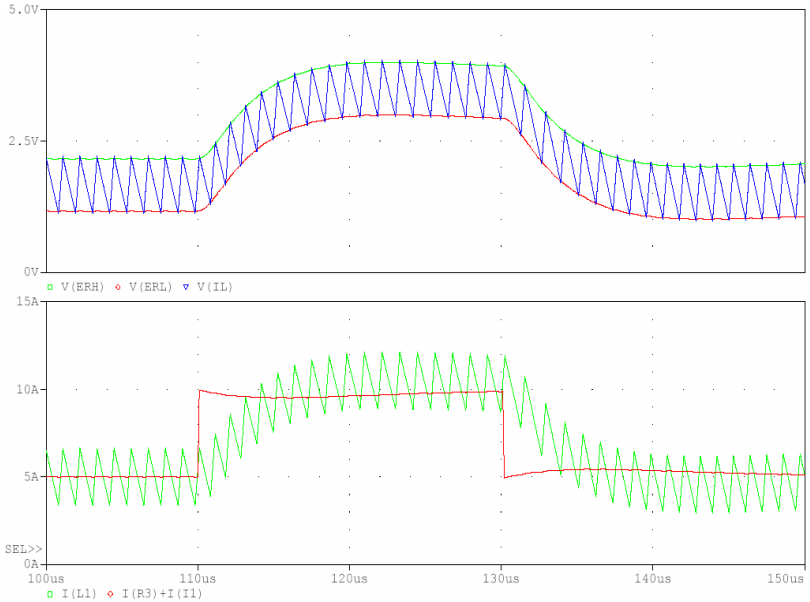
Switching frequency ~800kHz

Key waveforms

SIMPLIS



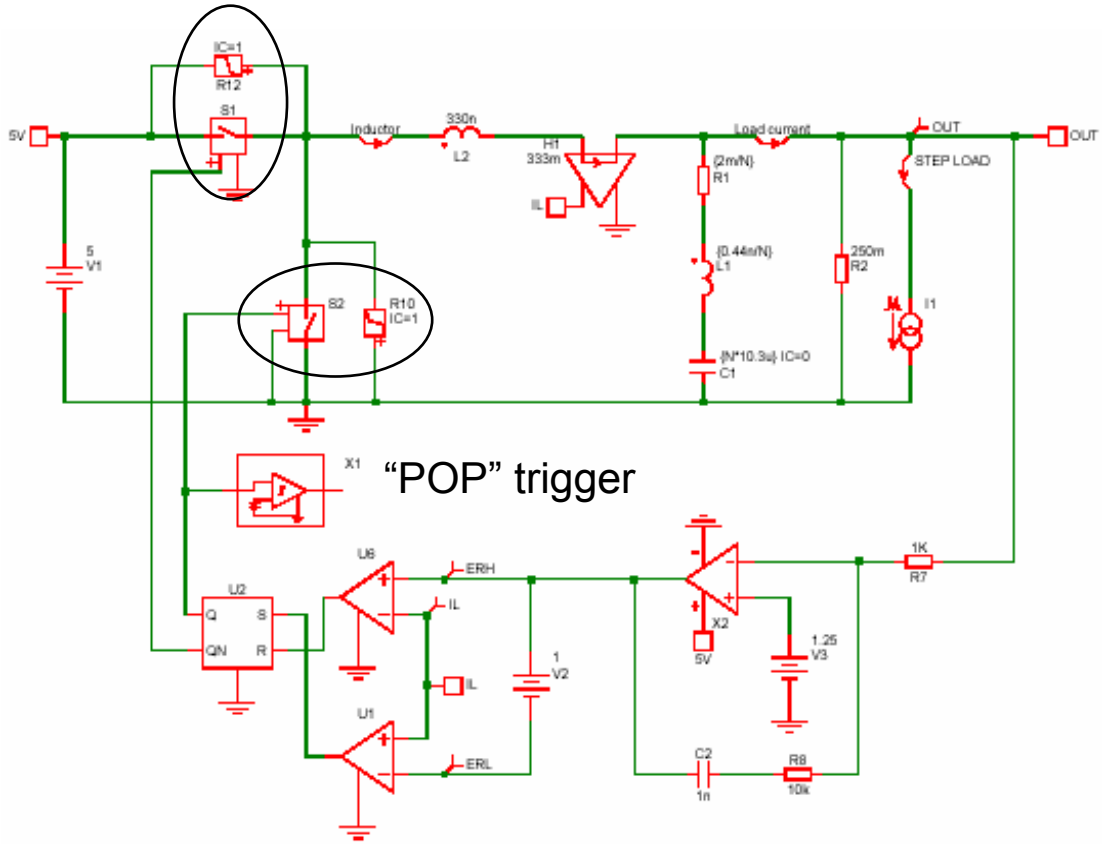
PSPICE



Transient response virtually identical

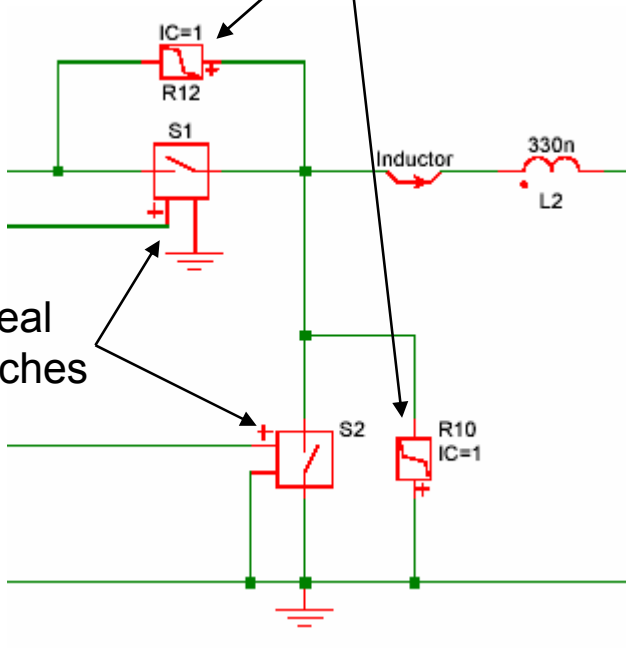
AC analysis with SIMPLIS

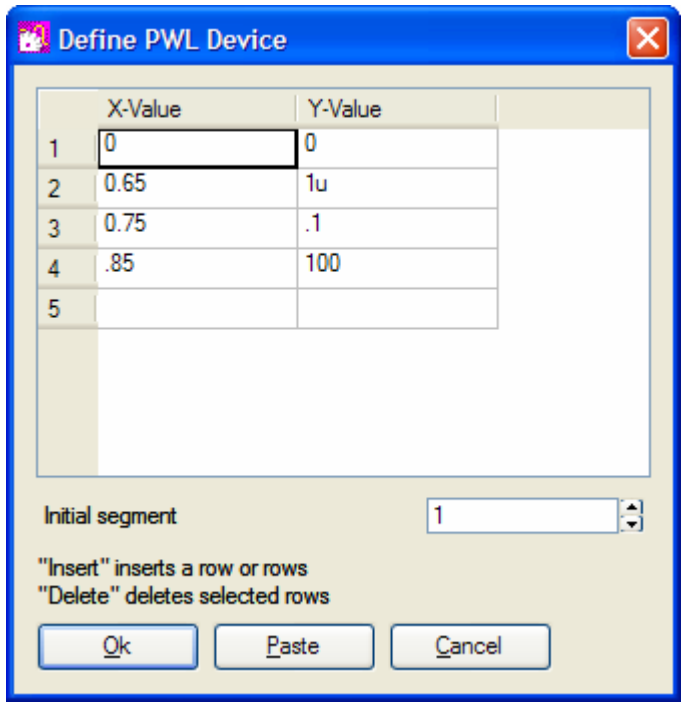
SIMPLIS model



MOSFETs replaced by ideal switch model

Piecewise-linear resistor represents body diode





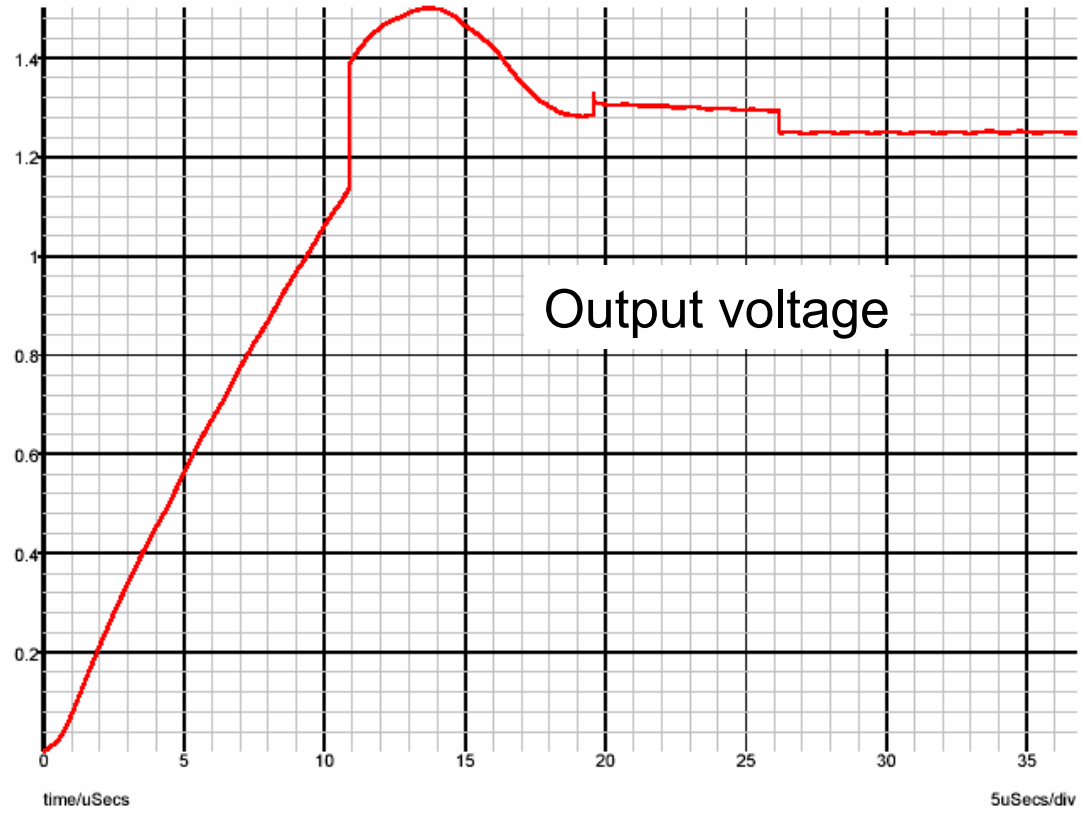
These simplifications have no effect on regulator dynamic performance

What does “POP” mean?

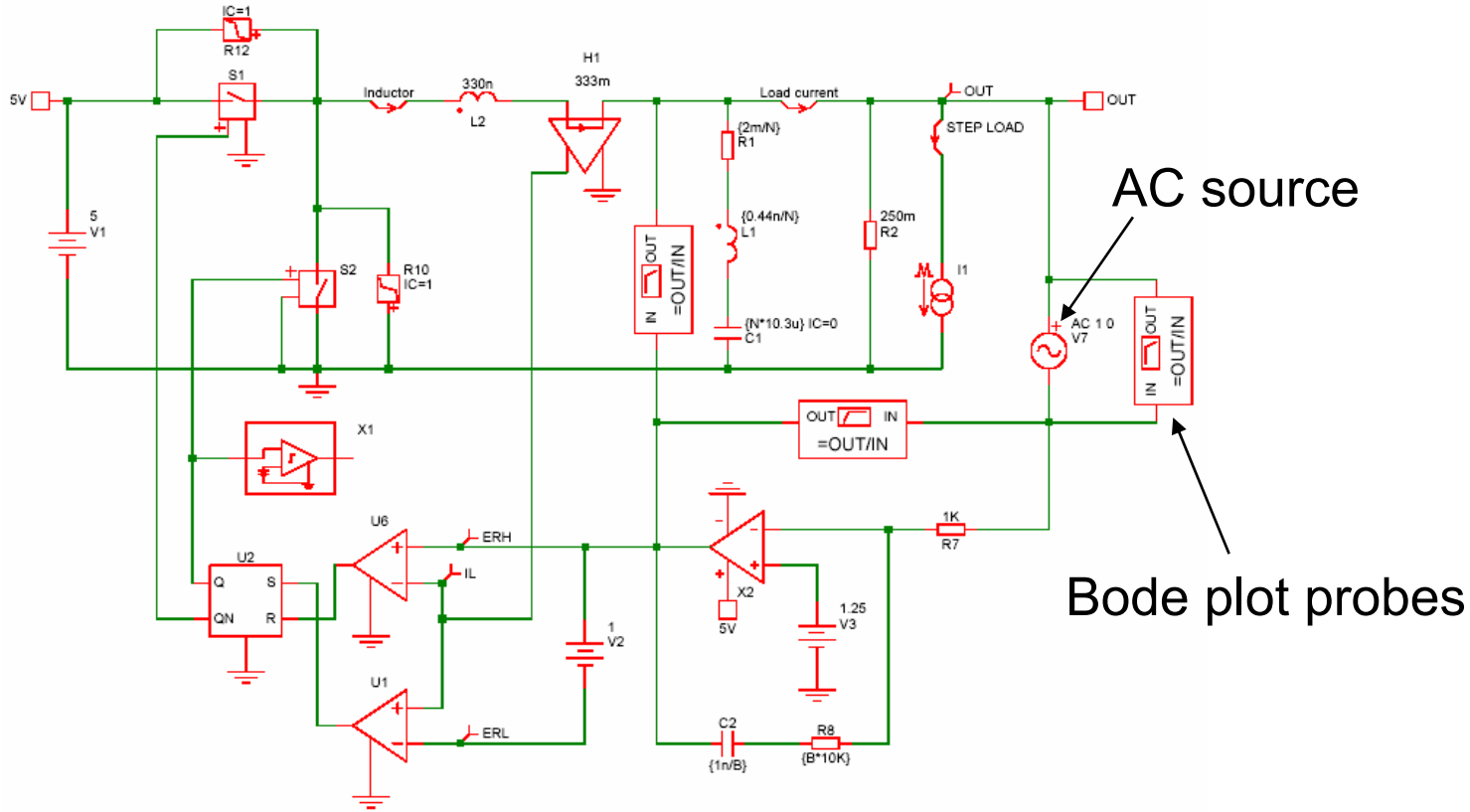
- POP stands for Periodic Operating Point Analysis
  - POP analysis rapidly locates the steady state operating point of a switching system without having to simulate the startup transient conditions. This considerably speeds the study of effects such as load transients.
  - Unlike the static methods used in SPICE, this analysis mode emulates a frequency sweep measurement as might be conducted on real hardware producing gain and phase plots without having to derive averaged models.

(excerpted from http://www.transim.com/SS_simplis.html)

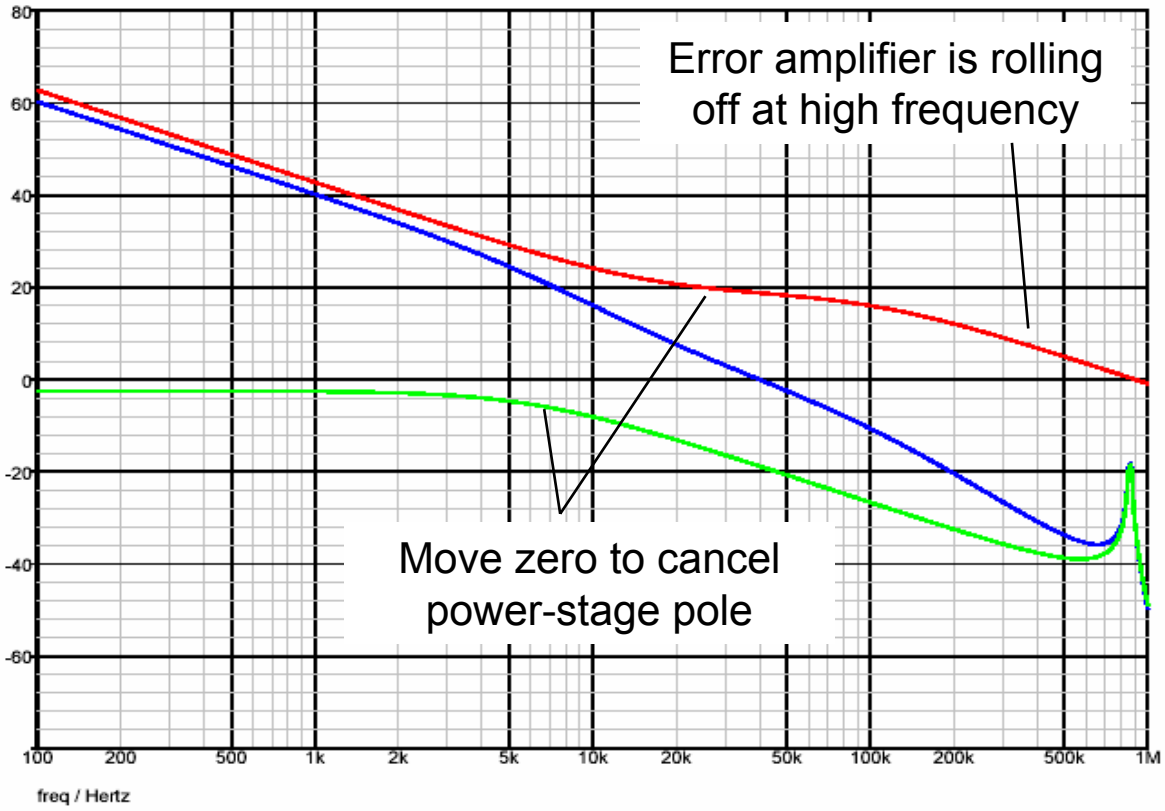
POP algorithm finding periodic steady state



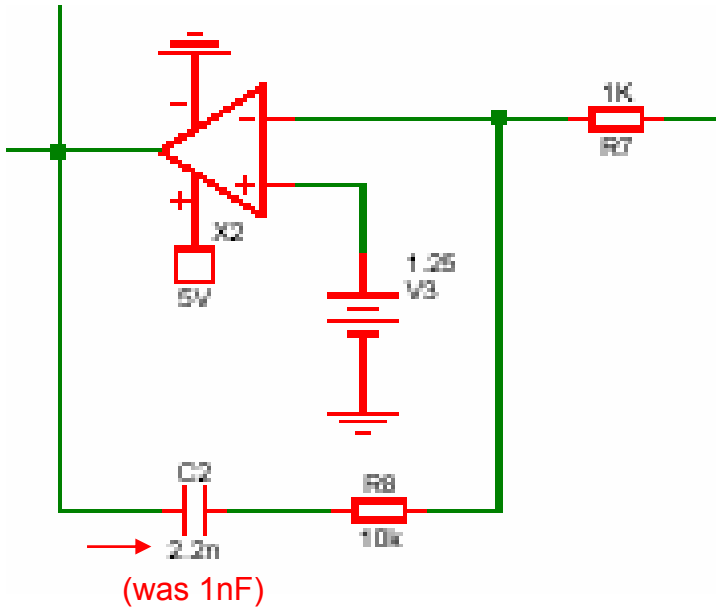
Add AC source to measure loop gain



Loop gain

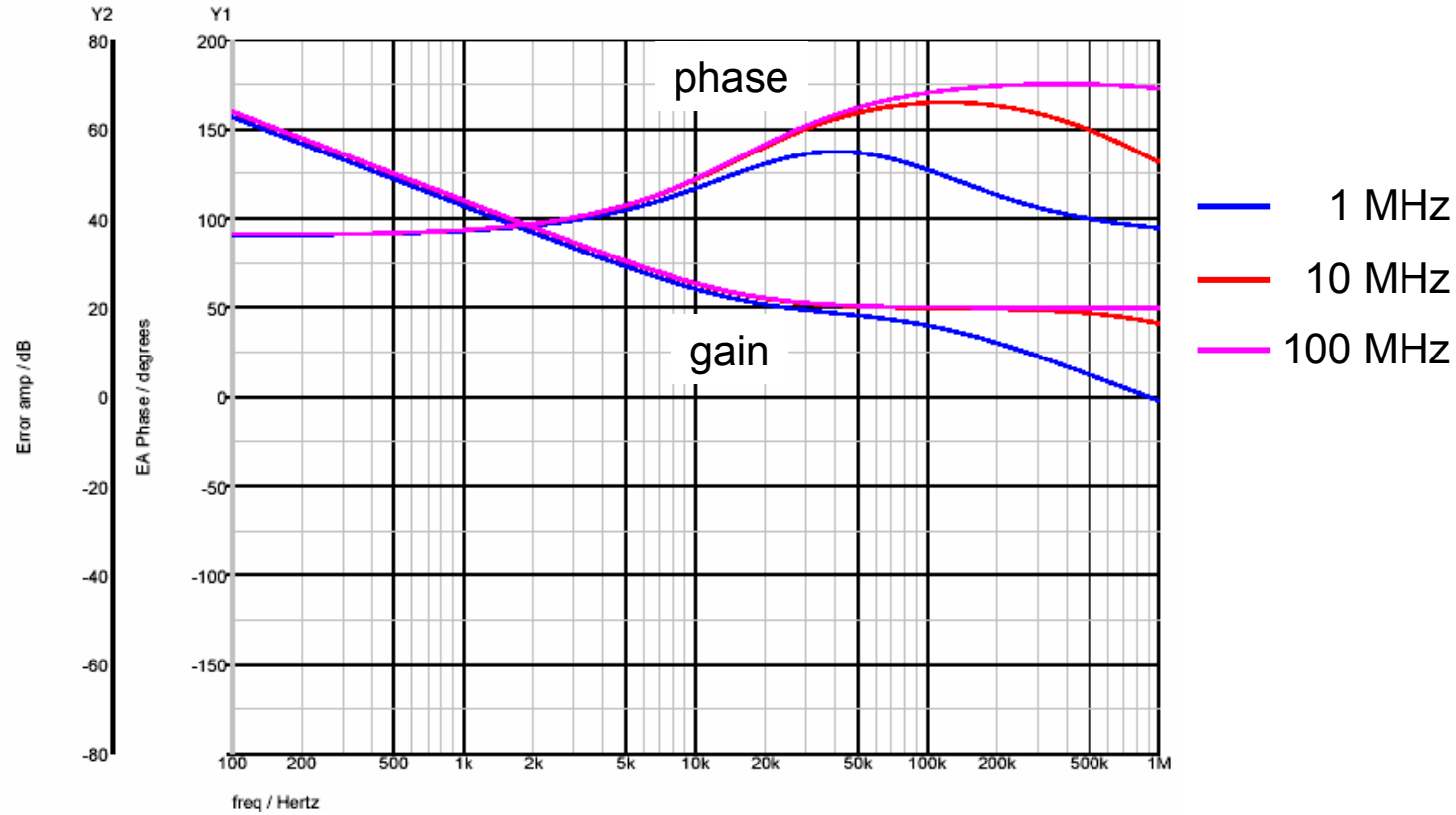


Move zero to match power stage

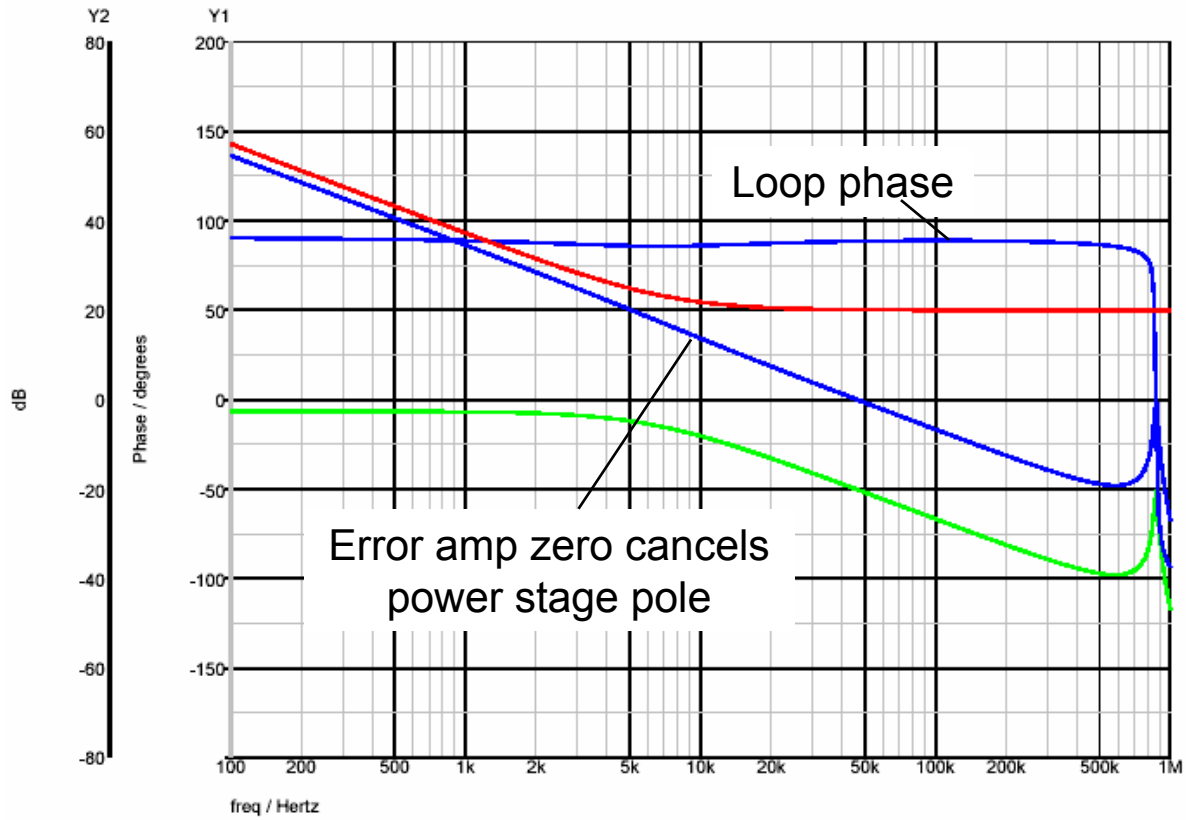


Zero moves from 15.9kHz to 7.2kHz

Compensator gain and phase vs op amp GBW



Updated Loop gain



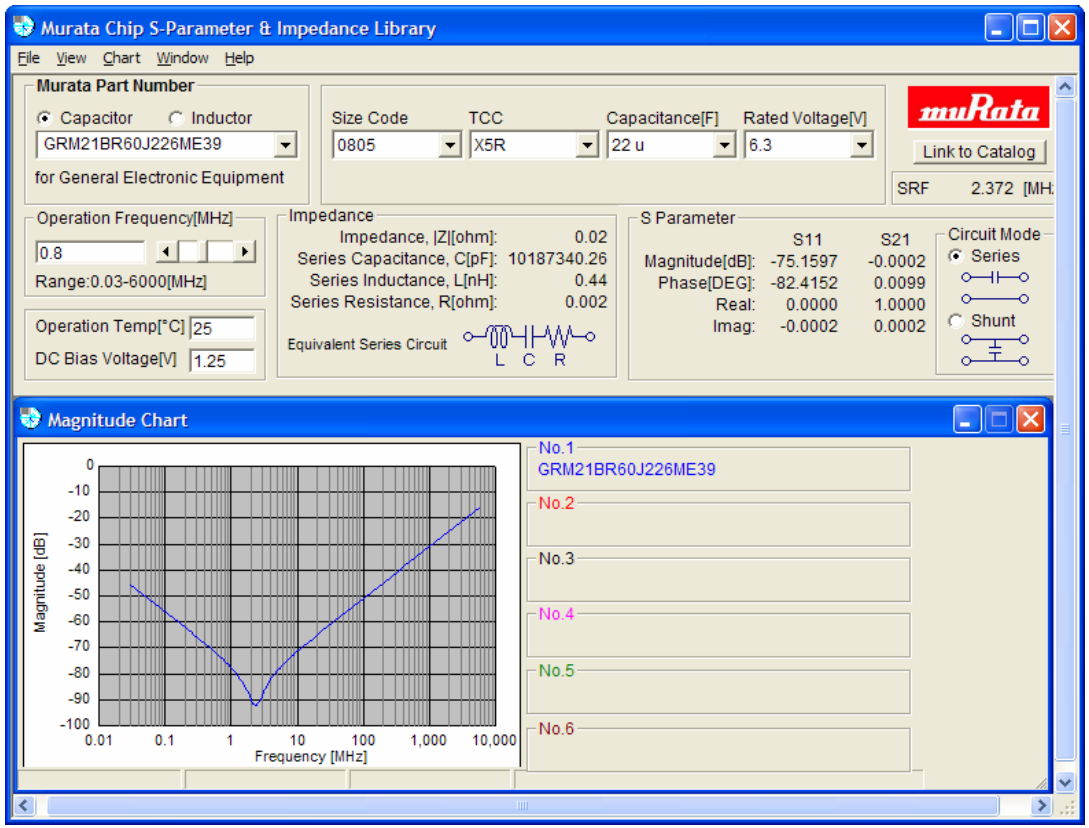
Step response

22uF 0805 X5R decoupling cap model:

C=10.2uF

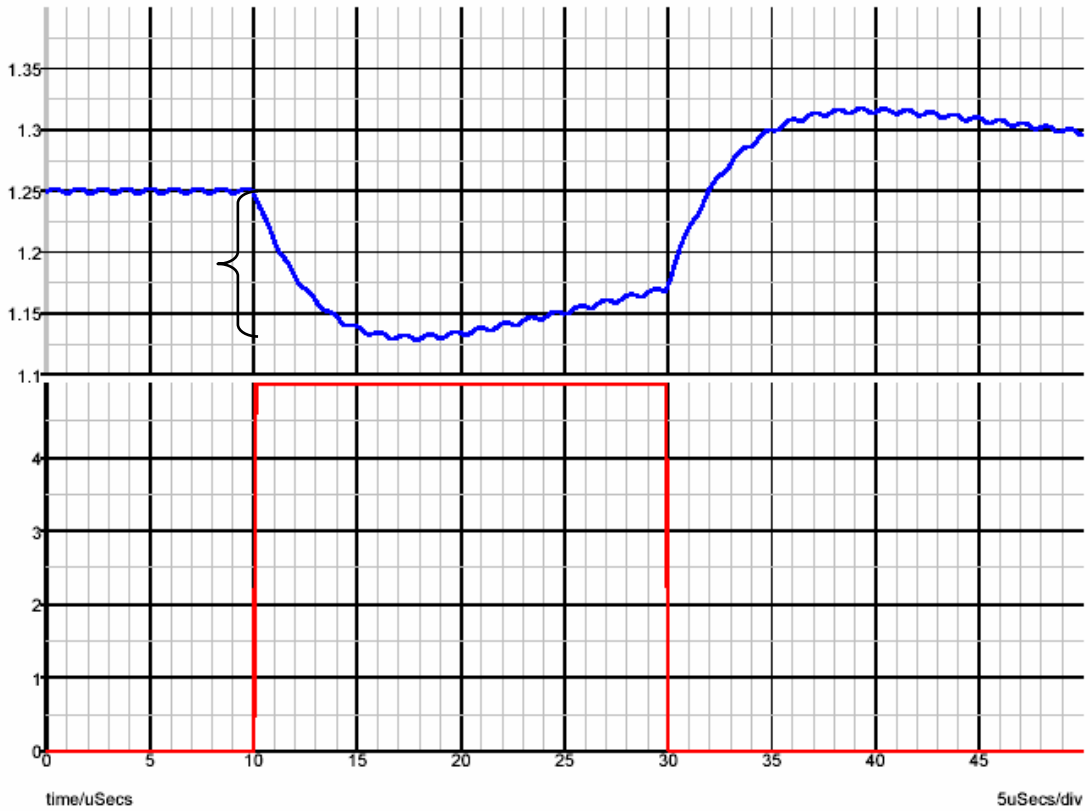
R=2mΩ

L=0.44nH



Impedance @ 1.25V & 800kHz

Step response with 10 caps

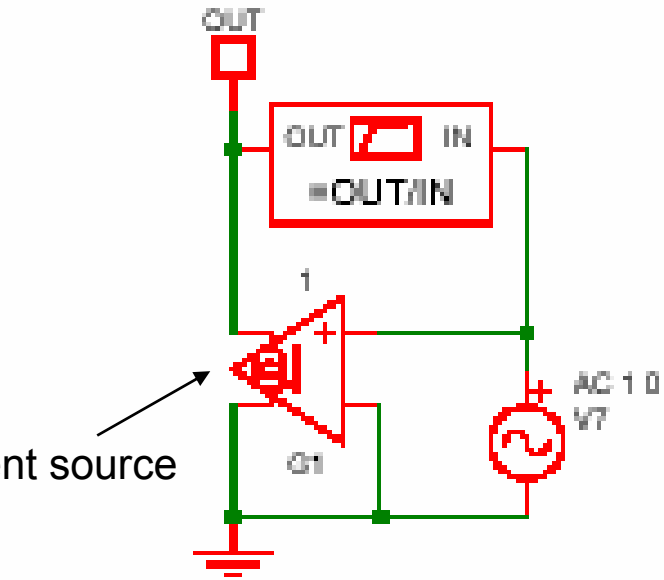


ΔV = 10% → needs improvement!

Output impedance

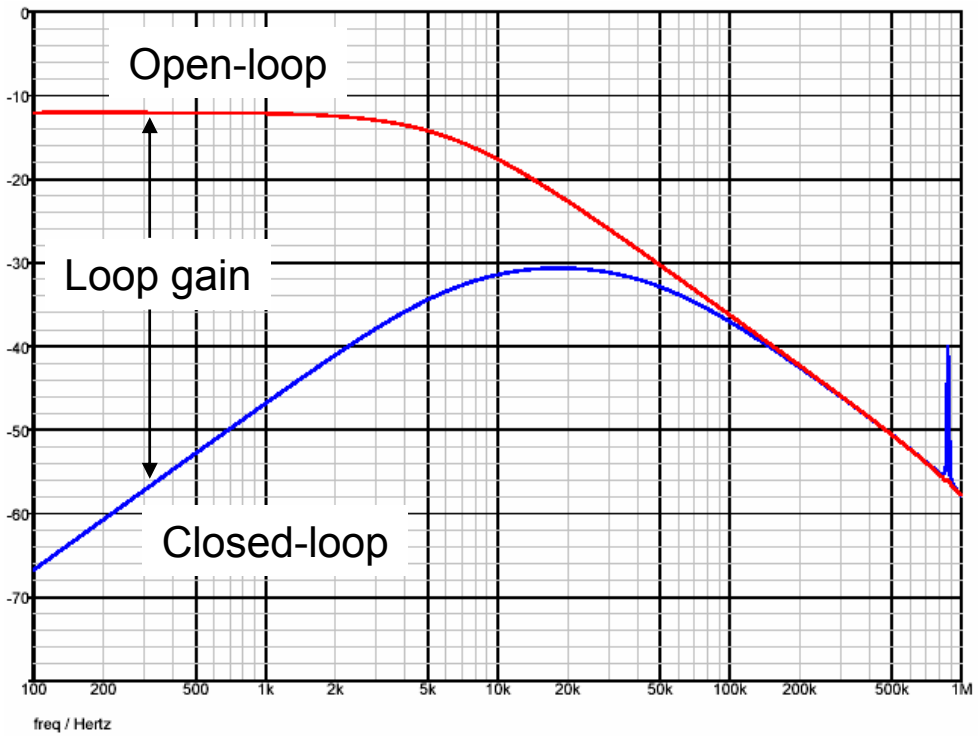
Measuring output impedance

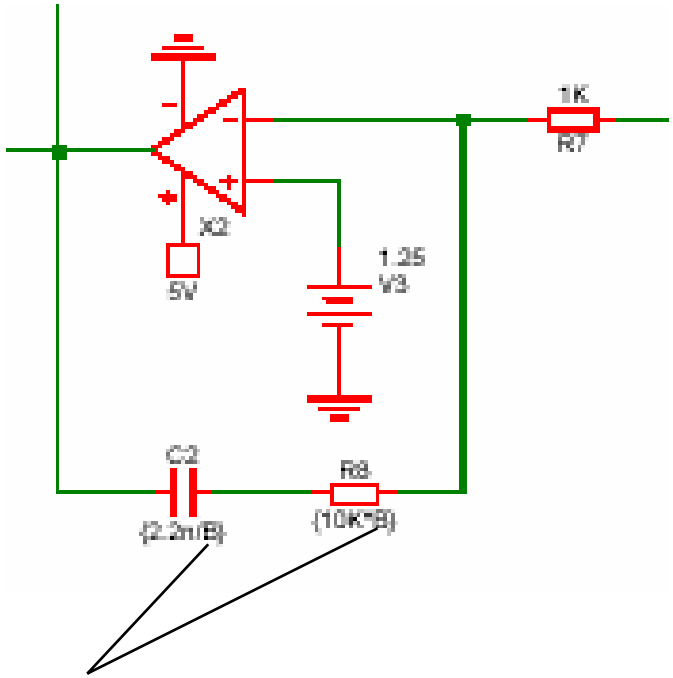
- Inject AC current into output
- Convert AC voltage source to AC current source



Unity-gain voltage-controlled current source

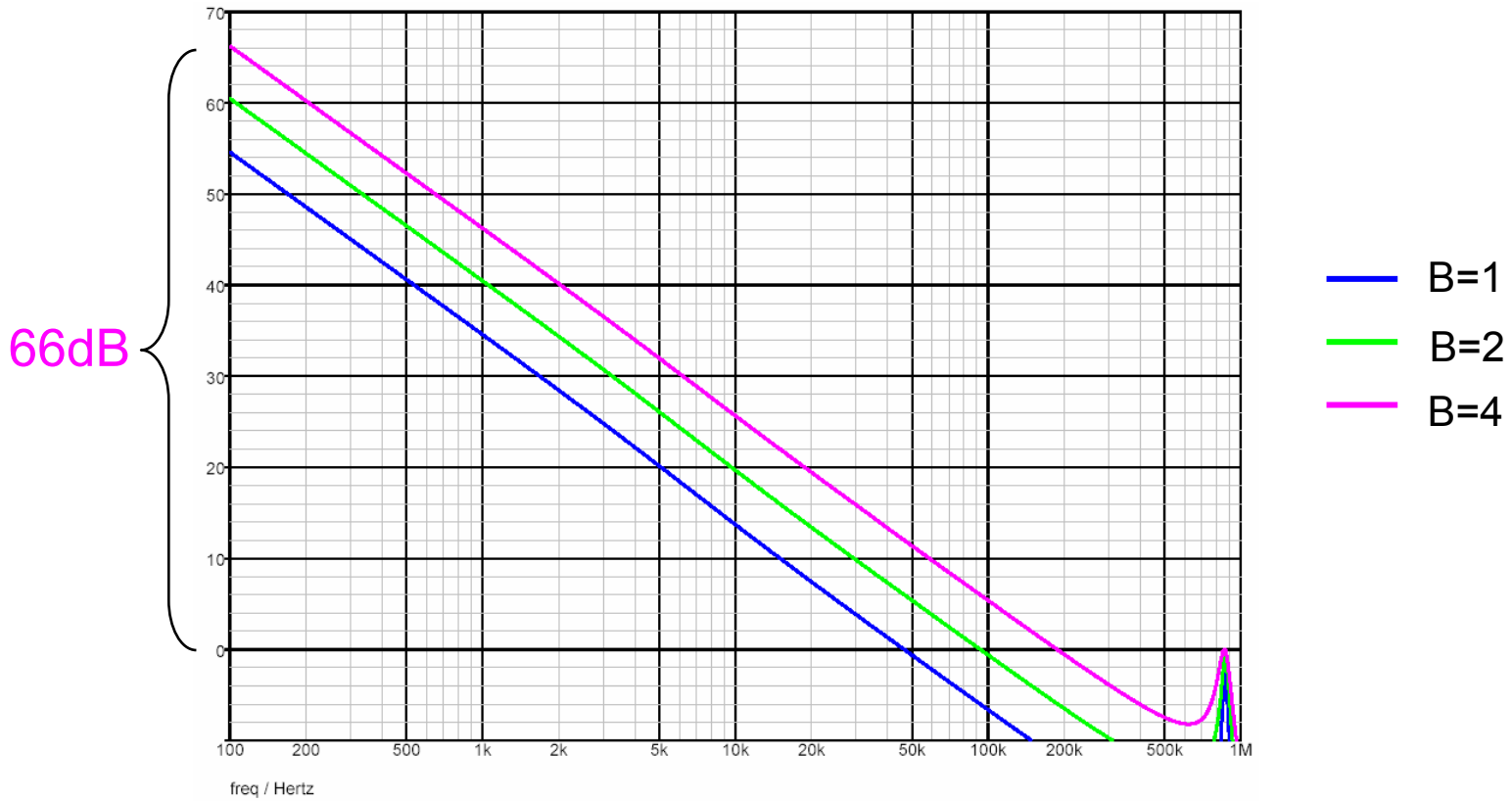
Open- and closed-loop output impedance



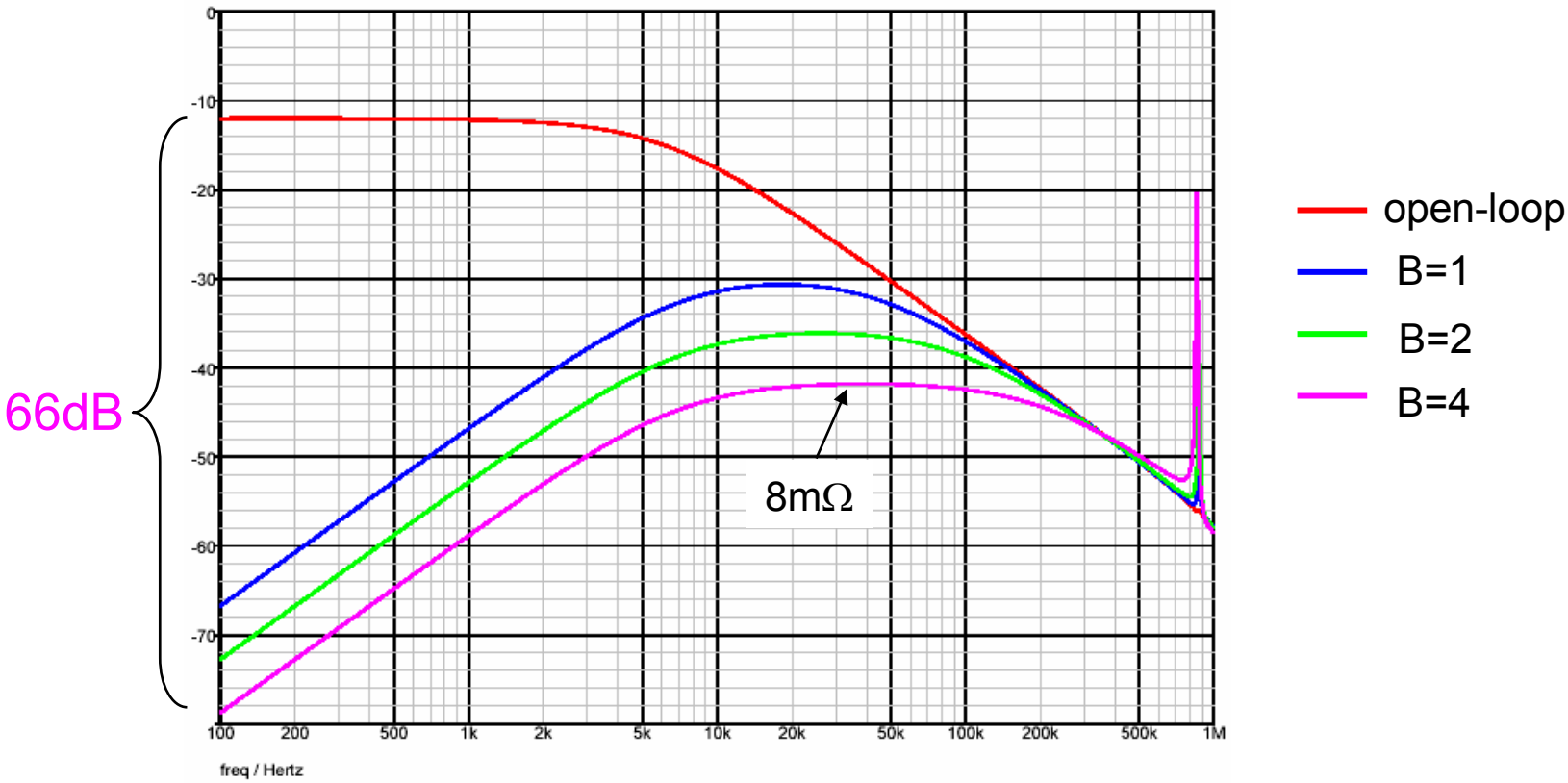


Parameter B: adjusts gain without moving zero

Loop gain vs B

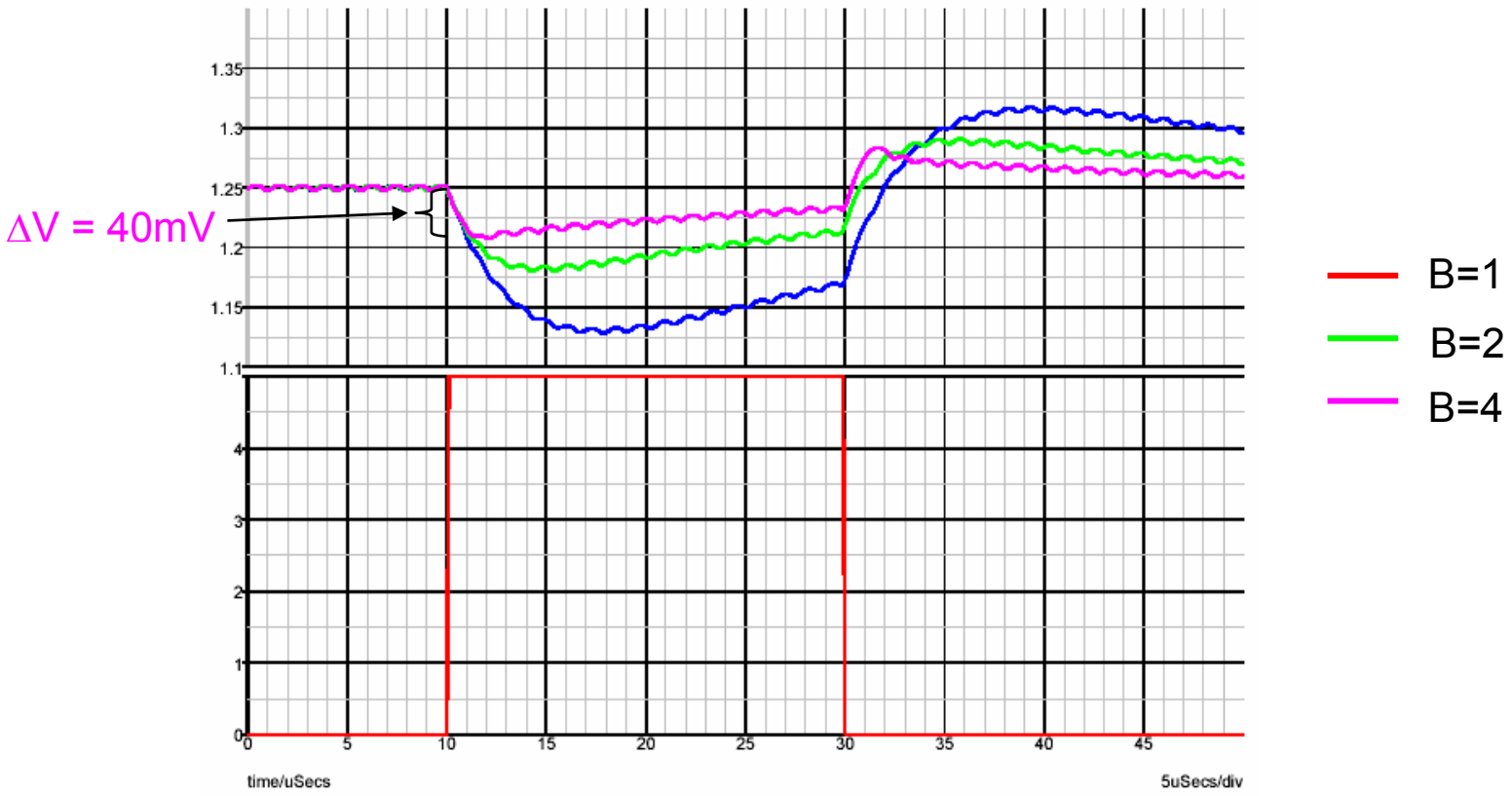


Output impedance vs loop gain



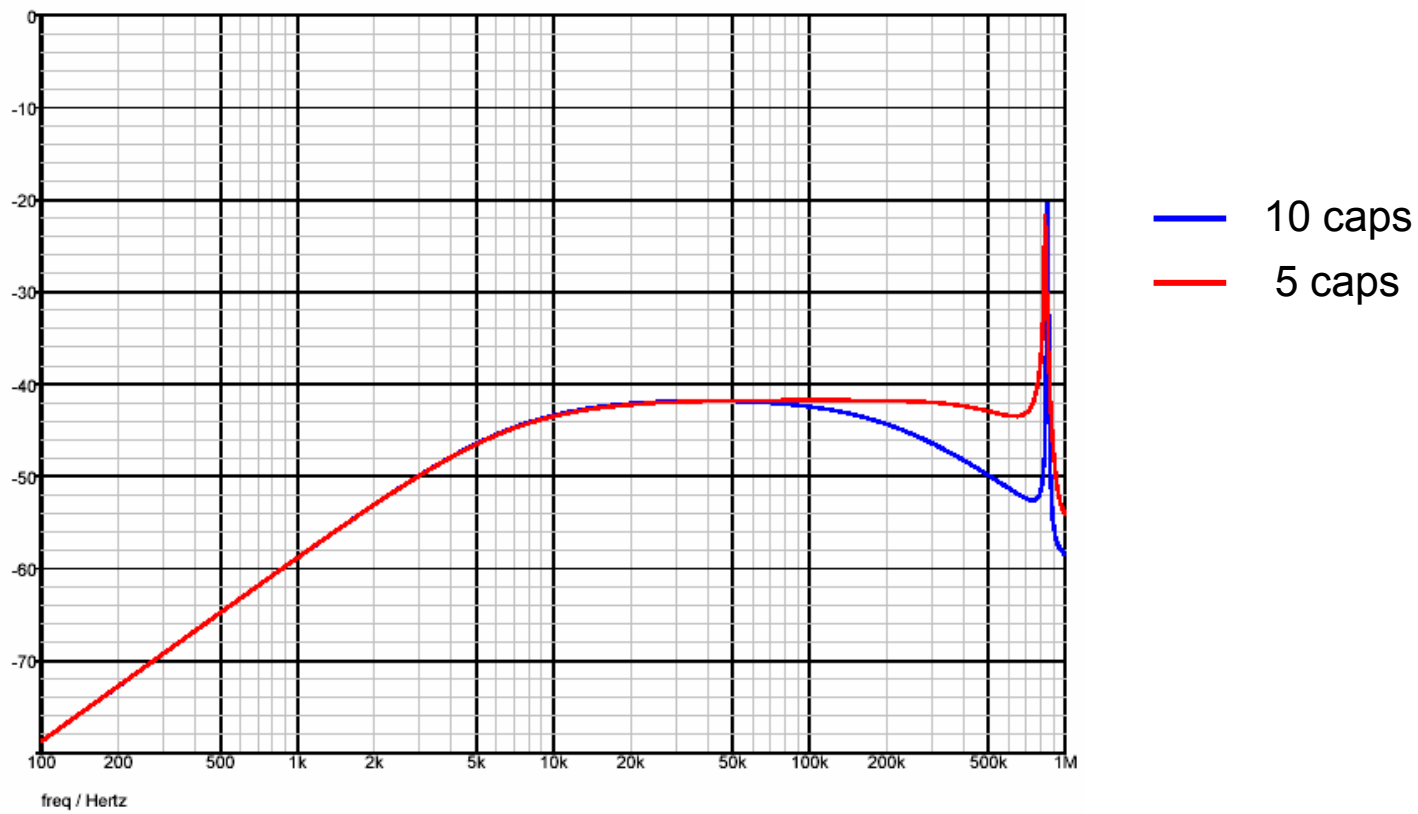
$$Z_{CL} = Z_{OL} / (1+\text{loop gain})$$

Step response vs loop gain



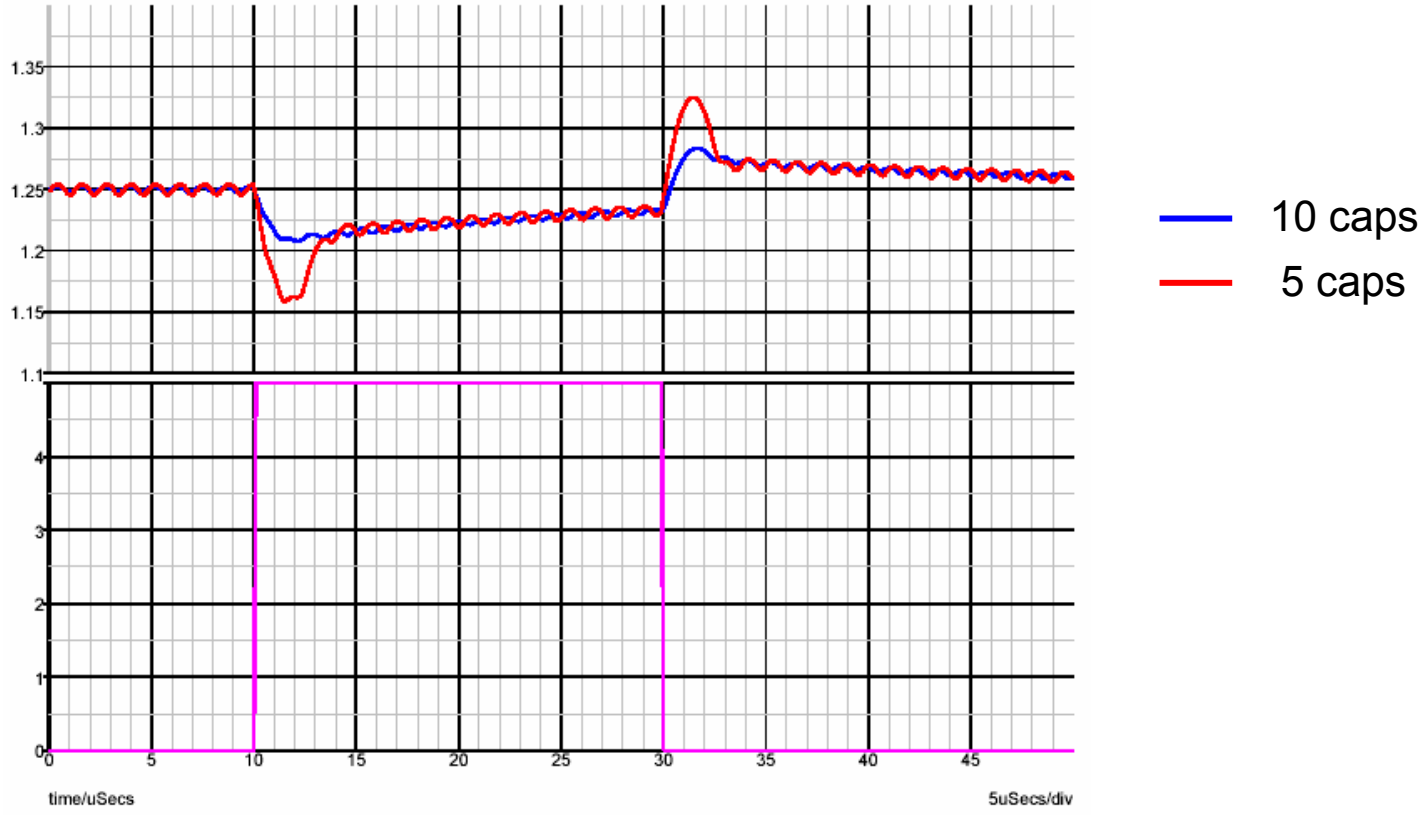
8mΩ x 5A= 40mV → excellent agreement!

Can the number of output caps be reduced?



Peak output impedance the same with 5 or 10 caps

Step response vs number of output caps

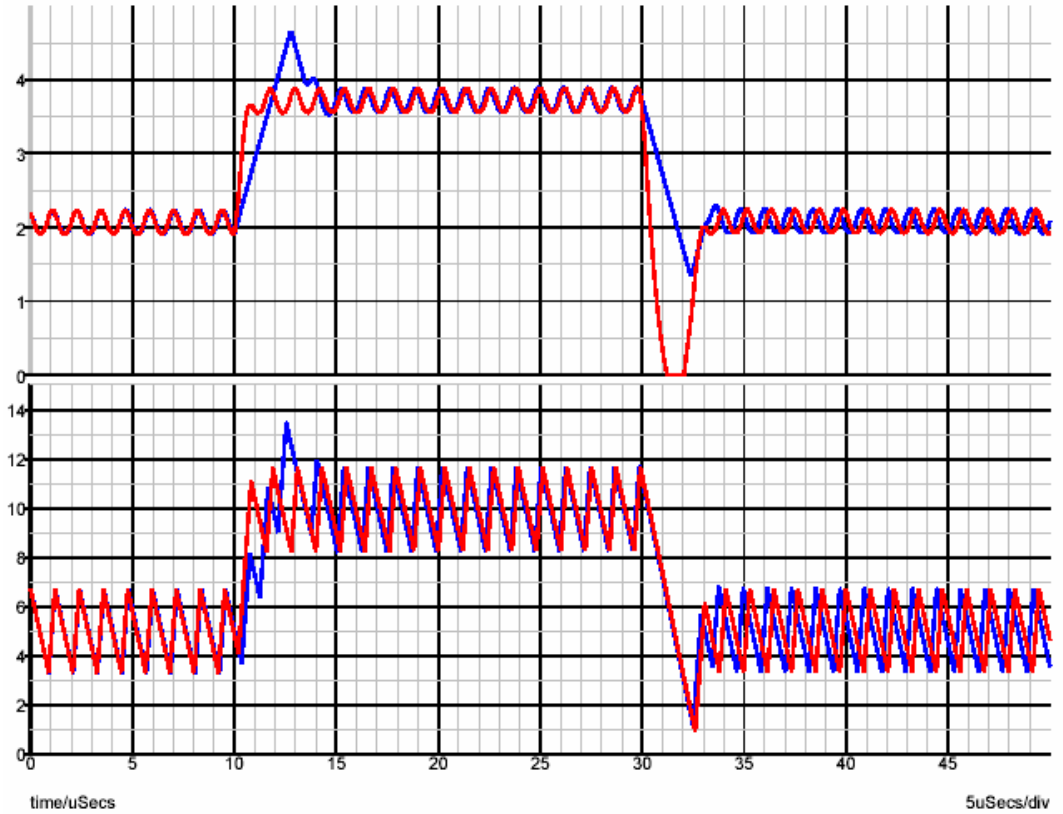


What's causing the overshoot?

Slew rate limiting of error amp!

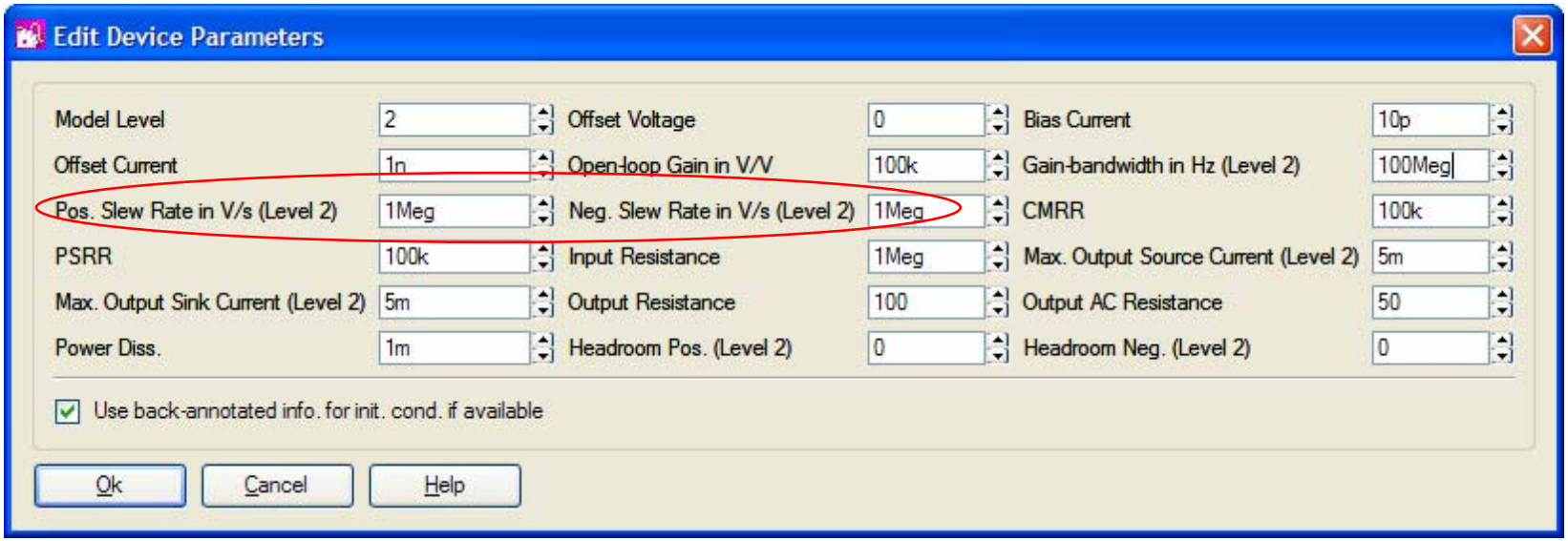
Error voltage

Inductor current



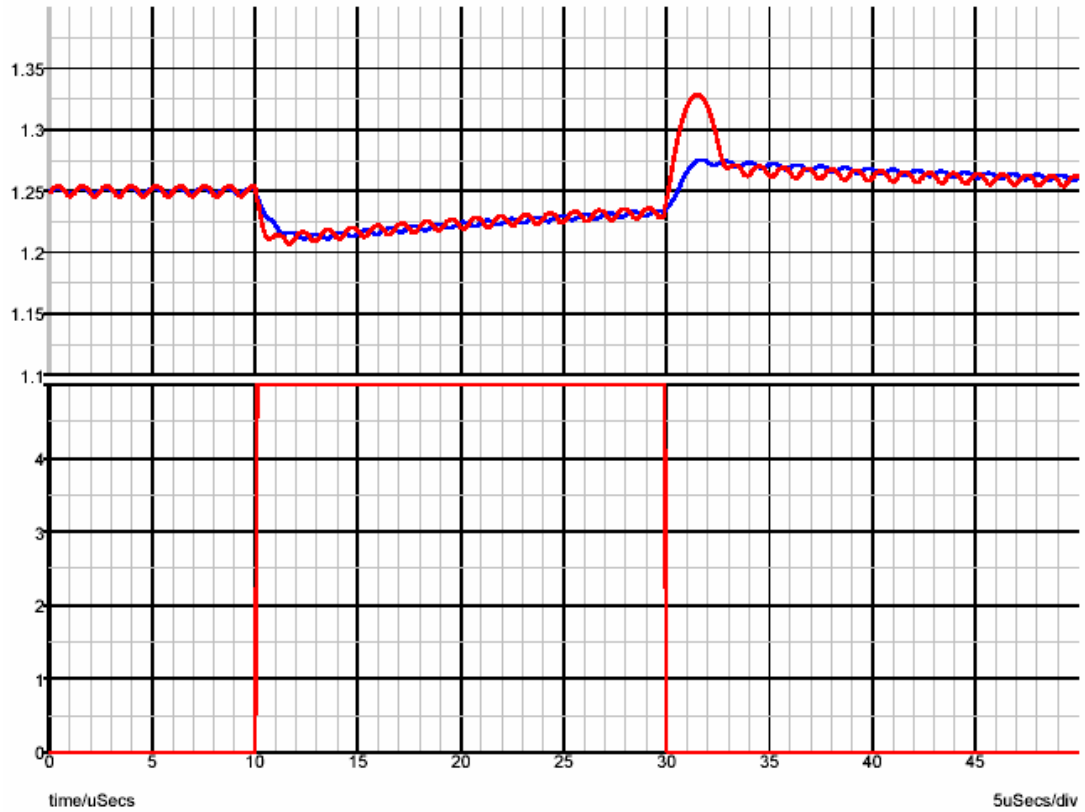
Transient response was limited by 1V/us max slew rate

Parameterized op amp



I forgot to adjust SR when I increased GBW (again!)

Step response with 5V/us amplifier



Power stage cannot slew fast enough in negative direction

Summary

- Difficult to size decoupling with all ceramic or low-ESR electrolytic caps
  - Computer modeling is essential to predict the regulator response to sudden load changes
  - SPICE is OK for simulating transient behavior, but AC analysis not possible with switching model
  - SIMPLIS provides both transient and AC analysis with the same model
  - Relatively easy to size decoupling once loop gain can be observed and the compensation optimized

Thank you!