A NEW SIMULATION METHOD OF LOSS ESTIMATION IN POWER FACTOR CORRECTION CONVERTERS

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Abstract - Loss analysis in a power factor correction AC-to-DC converter is often difficult to predict. One concern is finding a correct MOSFET simulation model. Another is the time-consuming aspect of doing simulation over a whole line cycle to determine MOSFET loss. This paper discusses a new simulation method that approximates the sinusoidal AC input voltage as a six-step DC input voltage in the simulation in order to significantly reduce the simulation while continuing the accurate loss estimation. Simulation results and comparison of time consumed are given.

I. INTRODUCTION

Assessment of advantages and disadvantages of switching power converters becomes increasingly important as more and more new circuit topologies come out. Loss estimation plays an important role in the evaluation of different topologies when assessing efficiency.

The switching loss of power switching devices is often difficult to predict. The unpredictable switching voltage and current waveforms during turn-on and turn-off times make switching loss estimation difficult if we only use the mathematical tools to do the estimation. For Power Factor Correction converters, it is even more difficult to estimate the switching loss, because the current in the switching device varies with the line voltage. Simulation is an important tool for determining switching loss.

In order to get accurate loss estimation in simulation, a good MOSFET model is needed. Almost every simulation tool has its own models for MOSFET. Spice-based simulation tools (such as Pspice or Saber) include very complex and detailed MOSFET models in their libraries. For piecewise linear simulation tools (such as Simplis), effort has been made and a modeling approach has been approved to accurately model the MOSFET for loss analysis.

Another issue of concern in loss estimation is the time we spent to obtain results. Designers can not afford to spend hours of time just to test one switching loss condition. Time is a real concern in product prototype test. For Spice-based simulation tools, the MOSFET model is very detailed and complex, but the simulation time is too long because of those complicated models. For piecewise linear simulation tools like Simplis, the fast algorithm helps to reduce simulation CPU time. But in Power Factor Correction converters, the situation is a little bit different. First it is necessary to run several line cycles to get the converter into steady state, and then a half line cycle must be run to get the loss estimation. So in order to obtain the loss estimation, several line cycles simulation time is required, which means a very long simulation CPU time, even for the fast piecewise linear simulation tools.

The purpose of this paper is to present a simulation approach for doing loss analysis in Power Factor Correction converters. Because of its fast speed and other attractive features, Simplis, a piecewise linear simulation tool, is chosen. By changing the sinusoidal input voltage into several DC steps, and using one of the nice features of Simplis----Periodic Operating Point (POP) analysis to accelerate the process of finding steady state, the simulation CPU time is reduced to a practical range. This paper uses a CCM boost Power Factor Correction converter as an example, and it is shown in figure 1. The MOSFET used in the circuit is IRFP450. Section II gives a brief introduction to modeling IRFP450 in Simplis. Section III presents the new simulation approach of changing the sinusoidal AC input into six-step DC input. Section

IV shows the simulation results. The advantages offered by the new approach are discussed in Section V.

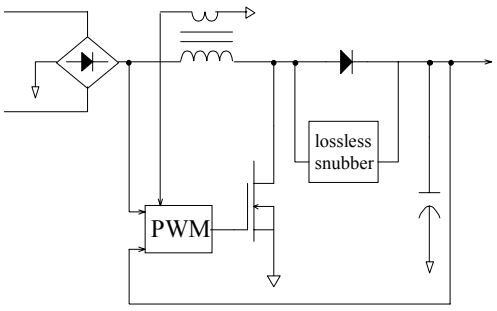

Figure 1. Power Factor Correction converter

II. MOSFET MODEL FOR IRFP450

The model of the IRPF450 MOSFET used in simulating the Power Factor Correction boost converter is shown in Figure 2. The model is purposefully simple for two reasons. First, simplicity of device models promotes an intuitive understanding of the basic operation of the MOSFET during the switching transitions. Second, simplicity reduces the CPU time required by the simulation engine to perform the analysis.

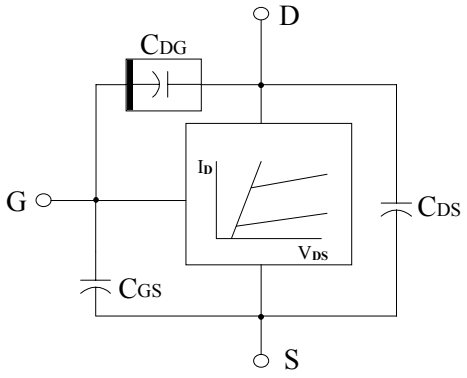

Figure 2. IRFP450 model for Simplis

As stated in the data sheets for the IRPF450 MOSFET, the capacitance Cdg varies greatly with the magnitude of the drain-to-gate voltage. This capacitance is modeled with inflection points at drain-to-gate voltages of 6V and 24V. The capacitance is 3300pF for drain-to-gate voltages less than 6V, 1200pF for voltages between 6V and 24V and 30pF for voltages greater than 24V. This approximation keeps the simulation time very reasonable, yet still yields drain voltage and current waveforms that closely approximate those observed in the actual circuit. The data sheets for the IRFP450 show that the capacitance between gate and source does not vary significantly as a function of drain to gate voltage. Hence, capacitance Cgs is a fixed value of 2500pF in the model.

The rectangular element in Figure 2 represents the piecewise linear model of the power MOSFET. During the OFF state, the transistor is modeled as a constant resistance Ro=2Mohm. During the ON state, the relationship between the drain voltage Vds and drain current Id is characterized as a constant resistance Rdson=0.4ohm. We model the transistor as a voltage-controlled current source parallel with the fixed resistor Ro when the MOSFET is in the active region of operation. The magnitude of the current in the current source is equal to the forward transconductance gm times the difference n potential between the gate voltage Vgs1 and the drain-to-gate voltage, Vgs(th). The value of Cdg versus drain-to-gate voltage, gm, Vgs(th) and Ro can be readily obtained from the data sheets for the MOSFET.

III. NEW APPROACH FOR LOSS ANALYSIS

In this section, the new approach for loss estimation in a Power Factor Correction converter is presented in detail. Before beginning the discussion, an important feature of Simplis needs to be introduced. Simplis' Periodic Operating Point (POP) Analysis actually inspired the idea of changing sinusoidal AC input into DC step input.

The Periodic Operating Point (POP) Analysis in Simplis uses a special algorithm to accelerate convergence to the steady-state for a periodic-operation system, so the converter can reach the steady state much faster than it would by a brute force simulation. For DC/DC converters, this feature offers huge benefit for simulation. But because of the variable input line, POP analysis can not be directly applied to Power Factor Correction converters.

But if POP analysis can be used in loss estimation for Power Factor Correction converters,

the simulation CPU time will be significantly reduced. This opportunity led to the idea that the sinusoidal AC input voltage can be changed into several steps of DC input voltages. For each of the steps, POP analysis is used on one DC input to quickly find steady state and do loss estimation. Figure 3 shows how to change the sinusoidal AC voltage into six-step DC voltage.

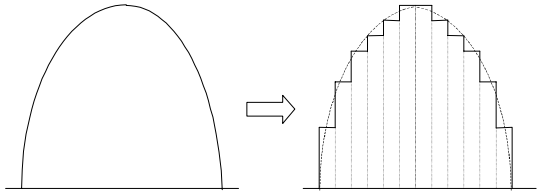

Figure 3. changing sinusoidal AC input into six-step DC input

The PFC circuit is shown in Figure 1, with an input line frequency of 60Hz, which means 4.167ms for a quarter line cycle. Each quarter line cycle is divided into six intervals as shown in Table 4. For each time interval ΔT, one DC value replaces that portion of sinusoidal wave. The simulation results for loss estimation are shown in Table 4(a) and (b).

Table 4(a). High input line 212Vac condition

Time Interval	Vin (DC)	Loss (DC)
(0ms, 0.695ms)	39V	0.873W
(0.695ms, 1.389ms)	114V	3.607W
(1.389ms, 2.084ms)	182V	5.074W
(2.084ms, 2.778ms)	237V	6.470W
(2.778ms, 3.473ms)	276V	7.504W
(3.473ms, 4.167ms)	296V	8.059W
Average Loss		**5.265W**

Table 4(a) shows that at high input line 212Vac condition, the six steps DC inputs are as follows: 39V, 114V, 182V, 237V, 276V and 296V. For each step, the MOSFET loss is shown in Table 4(a). The average MOSFET loss over a line cycle is 5.265W, which is only 0.4% different from the result of sinusoidal AC input 5.244W. In low line 90Vac condition, Table 4(b) shows the loss estimation result of 16.529W, which is only 0.1% different from the result of sinusoidal AC input 16.509W.

Table 4-b. Low input line 90Vac condition

Time Interval	Vin (DC)	Loss (DC)
(0ms, 0.695ms)	17V	1.571W
(0.695ms, 1.389ms)	48V	8.999W
(1.389ms, 2.084ms)	77V	15.102W
(2.084ms, 2.778ms)	100V	20.839W
(2.778ms, 3.473ms)	117V	25.181W
(3.473ms, 4.167ms)	126V	27.479W
Average Loss		**16.529W**

These simulation results show that the six-step DC input approach gives a fair accurate loss estimation, compared to the sinusoidal AC input. But for six-step DC input, the time saving is a great benefit. The total simulation CPU time used for six-step DC input is 5 minutes and 48 seconds. For sinusoidal AC input, in order to get the converter into steady state, four line cycles is run before the half line cycle loss estimation. The total simulation CPU time needed for sinusoidal AC input is 28 minutes and 17 seconds, which is five times more than the proposed six-step DC input method.

IV. MORE TESTING RESULTS

In order to verify the proposed approach in a more general way, several different MOSFET switching conditions are modeled and simulated.

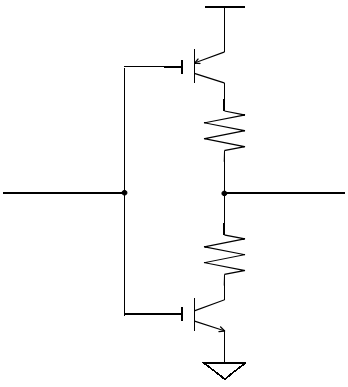

Figure 5. Gate driver for MOSFET

By changing the gate-driver resistor (shown in Figure 5), and with or without the snubber circuit, there are four possible MOSFET switching conditions: conduction loss dominant, turn-on loss dominant, turn-off loss dominant and both turn-on and turn-off loss dominant. For all of these four cases, results of both the DC step input and the sinusoidal AC input are listed in Table 6.

Table 6. Loss estimation comparison at different loss conditions

Case		1	2	3	4	CPU time
Gate Driver resistance	turn-on	5 ohm	47 ohm	5 ohm	47 ohm	
	turn-off	5 ohm	5 ohm	47 ohm	47 ohm	
Snubber		in	in	out	out	
Switching Loss Condition		conduction loss dominant	turn-on loss dominant	turn-off loss dominant	both turn-on and turn-off	
Loss (AC Input)		2.747W	5.120W	7.336W	9.486W	27 min 54 sec
Loss (DC Input)		2.784W	5.148W	7.386W	9.536W	5 min 26 sec
Error		1.3%	0.5%	0.7%	0.5%	

Table 6 shows that no matter how the MOSFET loss condition changes, the proposed six-step DC input still gives accurate results and save us lot of time.

V. CONCLUSIONS

The POP analysis in Simplis can achieve accurate steady state quite fast, which means the proposed six-step DC input approach allows the user to find the steady state quickly and accurately, whereas for sinusoidal AC input, sometime it's hard to determine exactly how many line cycles it takes to reach steady state. And for six-step DC input approach, once the steady state is found, only several switching cycles are needed for loss estimation, which will save us bunch of time and get us enough data points during switching transition.

By using the POP analysis of Simplis and replacing the sinusoidal AC input with six-step DC input, we can get the loss estimation fast enough and accurate enough.

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